AMENDMENTS TO THE CLAIMS

8. (Currently Amended) A transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate, the gate dielectric comprising:

a first dielectric material having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant,

the first and second dielectric materials being scalable for a set of feature size technologies,

the set of feature size technologies defined by a gate length in the range of 25-~~150~~ 70 nm, and

wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

9. (Original) The transistor of claim 8, wherein the second dielectric of the gate dielectric has a dielectric constant greater than the first dielectric constant.

10. (Original) The transistor of claim 8, wherein the first material of the gate dielectric has a first thickness and the second material of the gate dielectric has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of a length of the transistor gate.

11. (Canceled)

12. (Previously Amended) The transistor of claim 8, wherein the first gate dielectric material is selected from one of HfO_2 and ZrO_2.

13. (Original) The gate dielectric of claim 8, wherein the second dielectric material is ~~selected from one of BST and PZT.~~

14. (Original) The gate dielectric of claim 8, further comprising a third dielectric material having a third dielectric constant.

15. (Currently Amended) An apparatus comprising:

a semiconductor substrate having a transistor device formed thereon, the transistor device having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising:

a first dielectric material having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant,

the first and second dielectric materials being scalable for each of a plurality of feature size technologies, having a gate length in the range of 25~~-150~~70 nm, and

wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

16. (Previously Added) The apparatus of claim 15, wherein the second dielectric constant is greater than the first dielectric constant.

17. (Previously Added) The apparatus of claim 15, wherein the first material has a first thickness and the second material has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of the length of a transistor gate adapted to overly the gate dielectric.

18. (Canceled)

19. (Previously Amended) The apparatus of claim 15, wherein the first gate dielectric material is selected from one of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2.

20. (Previously Added) The apparatus of claim 15, wherein the second dielectric material is selected from one of BST and PZT.

21. (Previously Added) The apparatus of claim 15, further comprising a third dielectric material having a third dielectric constant.